

REMARKS

Reconsideration and allowance of this application are respectfully requested in light of the above amendments and the following remarks.

A new Abstract is submitted herewith as required by the Office Action.

The specification has been amended to overcome the objection thereto. As requested in the Office Action, the phrase "an test" has been replaced by "a test" throughout the specification. No new matter is introduced by the amendment of the specification.

The Applicant wishes to thank the examiner for the courtesy extended to Applicant's representative during a telephone interview on May 19, 2006. The interview discussion concerned the basis for the indefiniteness rejections applied to claims 1-11 and the best way for overcoming these rejections. The Examiner indicated that the claims were indefinite due to problems with the prose, grammar, and syntax used therein. The claims have been amended in accordance with this interview.

More specifically, claims 1-11 have been amended to avoid the issues underlying the objections and section 112, second paragraph, rejections applied to the original claims. Support for the subject matter of the new claims is provided at least in

the original claims, Figs. 3, 10, and 11, and the specification on page 14, lines 18-23.

In light of the above, reconsideration and withdrawal of the rejections under 35 USC 112, second paragraph, are respectfully requested

No prior art rejection was applied to original claims 2, 3, 5, 6, 10, and 11. Thus, the Applicant respectfully submits that these claims are directed to allowable subject matter. These claims have not been placed in independent form, because it is submitted that the independent claims are allowable for the reason set forth below.

Claims 1, 4, and 7-9 stand rejected, under 35 USC §102(e), as being anticipated by Ohtani et al. (US 6,421,286). The Applicant respectfully traverses based on the points set forth below.

The Office Action proposes that Ohtani discloses storing the address of a faulty memory cell and using the stored address to substitute an operational memory cell for the faulty cell (see Office Action page 7).

However, the Applicants respectfully submit that Ohtani fails to disclose or suggest the present claimed subject matter of a first data storage section that has different modes of operation during a first test mode for a test of the memory (BIST

operation) and a second test mode for a scan test. This subject matter may provide an advantage of reduction of hardware overhead.

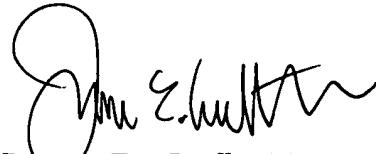
In contrast, Ohtani discloses a process wherein, at the time of carrying out the redundancy remediation procedure for plural memories having different capacities, with reduced surface area, the redundancy analysis function must be newly generated. In the present claimed invention, on the other hand, an existing circuit (first storage section for the scan test), is used for an additional purpose at the time of the redundancy analysis, thus achieving reduced surface area of the overall circuit.

Accordingly, the Applicant respectfully submits that Ohtani does not anticipate the subject matter defined by claim 1. Independent claims 4 and 7-9 similarly recite the above-mentioned feature distinguishing claim 1 from Ohtani, although claims 7 and 8 do so with respect to comparing row addresses of the faulty bit cells rather than column addresses, as recited in claim 1. Therefore, allowance of claims 1, 4 and 7-9 and all claims dependent therefrom is considered to be warranted for this independent reason.

In view of the above, it is submitted that this application is in condition for allowance and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



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JEL/DWW/att

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